REMARKS

Claim 1 calls for dynamically changing the number of bits stored per cell. The reference to Korsh mentions that different numbers of bits may be stored per cell in different regions of an array. See column 25, lines 32-35. It also mentions that when an N-bit per chip fails a test, it can be reconfigured as an N/2 or N/4 bit per cell chip. See column 25, lines 27-32.

However, neither of these citations set forth in the office action, teach dynamically changing the number of bits stored per cell. Each of these examples relate to the situation where the number of bits per cell is set. While the number of bits per cell may have been by design, N-bits in the second example, because of defects, it is reset in advance to N/2 bits per cell or N/4 bits per cell.

The number of bits stored per cell is not changed dynamically in the course of using the chip. Similarly, in the first example, it is stated that the system could be reconfigured, presumably in response to defects during testing and prior to use, when a portion of the memory operates with a different number of bits per cell than another. But, again, there is no ability to dynamically change the number of bits per cell. Instead, it appears that the chip is simply set to have different number of bits per cell in different regions.

Respectfully submitted,

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